AMENDMENTS TO THE SPECIFICATION

Page 6, please amend the paragraph beginning at line 31 and bridging pages 6 and 7 as follows:

As can be seen from Figs. 3 and 4, the depletion layer extends from P^--type semiconductor substrate 1 and ~~P^--type~~ impurity diffusion regions type P^- 4, P^+ 6, P^- 11, P^+ 12, P^+ 16, P^- 19, P^+ 22 and P^- 25, respectively, when the latch circuit is in the off-state; thereby, N^--type epitaxial layer 2 is completely depleted. Accordingly, the surface electrical field of N- type epitaxial layer 2 is relaxed.

Page 7, please amend the paragraph beginning at line 6 as follows:

Further, the depletion layer extending from P^--type semiconductor substrate 1 does not reach ~~P^--type~~ impurity diffusion regions type P^- 4, P^+ 6, P^- 11, P^+ 12, P^+ 16, P^- 19, P^+ 22 and P^- 25. Such an effect is an effect accompanying the structure of relaxing the surface electrical field referred to as DOUBLE RESURF, and is described in Japanese Patent Laying-Open No. 10-4143. The withstand voltage of the element becomes a one-dimensional withstand voltage in the direction perpendicular to the main surface of the semiconductor substrate if the DOUBLE RESURF condition for relaxing the surface electrical field is satisfied. Accordingly, the withstand voltage of the element is determined by the withstand voltage between P- type semiconductor substrate 1 and N^--type epitaxial layer 2.

Page 8, please amend the paragraph beginning at line 4 as follows:

Accordingly, a field P-channel IGBT (Insulated Gate Bipolar Transistor), instead of field PMOS 2, is formed in the right side of the semiconductor device of the present embodiment with source electrode V_{dd} 15 as the border. A forward bias (positive bias) generates between P^+-type

impurity diffusion region 18 and N^+-type impurity diffusion region 28 in this P-channel IGBT; thereby, an NPN transistor having N^+-type impurity diffusion region 28 as an emitter electrode functions. Thereby, the current is amplified to be multiplied by hFE by means of the NPN transistor.

Page 9, please amend paragraph beginning at line 9 as follows:

A P^--type impurity diffusion region 31 is formed in the vicinity of N^+-type impurity diffusion region 14. A P^+-type impurity diffusion region 32 is formed adjacent to P^--type impurity diffusion region 31. Further, an N^+-type impurity diffusion region 33 is formed inside P^+-type impurity diffusion region 32. A drain ~~An~~ electrode V_{out} 38 is connected to both P^+-type impurity diffusion region 32 and N^+-type impurity diffusion region 33. Further, a P^+-type impurity diffusion region 34 is formed at a predetermined distance away from the side of P^+-type impurity diffusion region 32.

Page 9, please amend the paragraph beginning at line 30 and bridging pages 9 and 10 as follows:

Field PMOS 2 and an NMOS (N Channel Metal Oxide Semiconductor) 4, as high side switches of a latch circuit, also share P^+-type impurity diffusion region 12 and N^+-type impurity diffusion region 14, which are connected to source electrode V_{dd} 15, as well as ~~P+~~ P^--type impurity diffusion region 31 in the above described semiconductor device of the present embodiment. Accordingly, the area of the element formation region in a plane parallel to the main surface of semiconductor substrate 1 can be reduced. As a result, the semiconductor device can be miniaturized even by means of the semiconductor device according to the present embodiment.